WHAT IS CLAIMED IS:

1.   A digital phase-domain phase-locked loop circuit comprising:

a digitally-controlled oscillator (DCO);

a gain element feeding the DCO and operational to compensate for DCO gain in response to a loop gain alpha multiplier signal;

an oscillator phase accumulator operational to accumulate DCO generated clock edges;

a reference phase accumulator operational to accumulate a frequency division ratio command and a modulating data signal and to generate an accumulated frequency control word (FCW) therefrom;

a phase detector operational to compare the accumulated FCW and the accumulated DCO generated clock edges and generate a filtered phase error in response thereto;

a loop gain alpha multiplier element operational to generate the loop gain alpha multiplier signal in response to a filtered direct modulator output signal; and

a direct modulator operational in response to the modulating data signal and the filtered phase error to generate the filtered direct modulator output signal.

2.   The digital phase-domain phase-locked loop circuit according to claim 1 wherein the direct modulator comprises:

a loop gain alpha inverse multiplier element operational to generate a signal in response to the modulating data signal; and

a combinational element feeding the loop gain alpha multiplier element in response to the signal generated by the loop gain alpha inverse multiplier element and further in response to the filtered phase error.

.. .. operational to selectively attenuate a feed-forward path associated with the phase-locked loop circuit.

4.   The digital phase-domain phase-locked loop circuit according to claim 1 further comprising an all-pass filter operational to pass a phase error generated via the phase detector to generate the filtered phase error.

5.   The digital phase-domain phase-locked loop circuit according to claim 1 wherein the gain element is operational to generate an oscillator tuning word that is a function of a reference frequency f_{ref} and an estimated DCO gain $\hat{K}_{DCO}$, wherein the function is defined by: $\dfrac{f_{ref}}{\hat{K}_{DCO}}$.

6.   A digital phase-domain phase-locked loop circuit comprising:

        a digitally-controlled oscillator (DCO);

        a gain element feeding the DCO and operational to compensate for DCO gain in response to a direct modulator output signal;
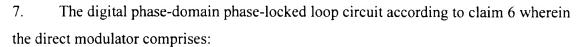
        an oscillator phase accumulator operational to accumulate DCO generated clock edges;

        a reference phase accumulator operational to accumulate a frequency division ratio command and a modulating data signal and to generate an accumulated frequency control word (FCW) therefrom;

        a phase detector operational to compare the accumulated FCW and the accumulated DCO generated clock edges and generate a filtered phase error in response thereto;

        a loop gain alpha multiplier element operational to generate a loop gain alpha multiplier signal in response to the filtered phase error; and

        a direct modulator operational in response to the modulating data signal and the alpha multiplier signal to generate the direct modulator output signal.

7.   The digital phase-domain phase-locked loop circuit according to claim 6 wherein the direct modulator comprises:

        a combinational element operational to combine the modulating data signal and the alpha multiplier signal.
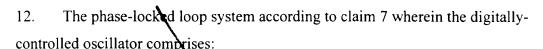
8.   The digital phase-domain phase-locked loop circuit according to claim 7 further comprising a direct modulation switch element operational to selectively attenuate a feed-forward path associated with the phase-locked loop circuit.

9.   The digital phase-domain phase-locked loop circuit according to claim 6 further comprising an all-pass filter operational to pass a phase error generated via the phase detector to generate the filtered phase error.

10.   The digital phase-domain phase-locked loop circuit according to claim 6 wherein the gain element is operational to generate an oscillator tuning word that is a function of a reference frequency f_{ref} and an estimated DCO gain $\hat{K}_{DCO}$, wherein the function is

defined by: $\dfrac{f_{ref}}{\hat{K}_{DCO}}$.

11.   A phase-locked loop system comprising:

        a digitally-controlled oscillator responsive to an oscillator tuning word (OTW) to generate an oscillator clock;

        a direct modulator operational in response to a modulating data signal and a filtered phase error to generate the OTW; and

        a phase-locked loop (PLL) operational in response to a channel selection signal and the modulating data signal to generate the filtered phase error.

12.   The phase-locked loop system according to claim 7 wherein the digitally-controlled oscillator comprises:

a voltage controlled oscillator; and

a digital-to-analog converter operational to generate an oscillator tuning voltage in response to the OTW.

13.   The phase-locked loop system according to claim 11 wherein the direct modulator comprises a combinational element feeding the digitally-controlled oscillator such that an oscillator gain can be compensated to substantially remove its effects on loop behavior.

14.   The phase-locked loop system according to claim 11 further comprising a direct modulation switch element operational to selectively attenuate a feed-forward path associated with the PLL.

15.   The phase-locked loop system according to claim 14 wherein a path through the direct modulator is defined by a transfer path gain between the modulation switch element and the digitally-controlled oscillator.

16.   The phase-locked loop system according to claim 15 wherein the transfer path gain is dependent upon a reference frequency f_{ref} and an estimated digitally-controlled oscillator gain $\hat{K}_{DCO}$, is functionally defined as $\dfrac{f_{ref}}{\hat{K}_{DCO}}$.

17.   The phase-locked loop system according to claim 11 wherein the PLL comprises a phase detector feeding an all-pass filter, wherein the phase detector is responsive to the channel selection signal and the modulating data signal to generate a phase error, and wherein the all-pass filter is operational to pass the phase error to generate the filtered phase error.

18.   A method of operating a digital phase-locked loop (PLL) comprising the steps of:

(a) providing a phase-locked loop including a digitally-controlled oscillator (DCO) having a gain K_{DCO}, and a phase detector, wherein the DCO is responsive to an oscillator tuning word (OTW) to generate a DCO output clock having a frequency f_r, and further wherein the phase detector is responsive to a channel selection signal, a modulating data signal and the output clock to generate a phase error;

(b) providing a direct modulator operational in response to the phase error and the modulating data signal to generate the OTW;

(c) observing an accumulated phase $\Delta\phi$ in the phase error in response to a given change Δx in the OTW; and

(d) estimating the DCO gain $\hat{K}_{DCO}$, defined by $\hat{K}_{DCO} = \dfrac{\Delta\phi}{\Delta x} \cdot f_{ref}$ such that a DCO gain can be compensated to substantially remove its effects on loop behavior.

19.   The method according to claim 18 further comprising the step of:

(e) repeating step (c) and step (d) a plurality of times to obtain an average value for the estimated DCO gain $\hat{K}_{DCO}$.

20.   The method according to claim 19 further comprising the step of:

(f) re-estimating the DCO gain $\hat{K}_{DCO}$, in response to changes in PLL operating parameters such that the DCO gain can be compensated to substantially remove its effects on loop behavior in response to the changes in PLL operating parameters.

21.   The method according to claim 18 wherein the accumulated phase $\Delta\phi$ in the phase error is generated via a fractional phase error correction process.